CLAIMS

What is claimed is:

1. An integrated circuit (IC) package comprising:

a substrate including an IC;

a ground line; and

an encoded region to provide information based upon selective deposition of solder balls electrically coupled to the ground line.

2. The package of claim 1, wherein the substrate is the substrate of a ball grid array (BGA) package.

3. The package of claim 2, wherein the IC is a processor.

4. The package of claim 3, wherein a deposited solder ball in a solder ball area of the encoded region is used to denote a logical "0", and an absence of a solder ball in the solder ball area is used to denote a logical "1".

5. The package of claim 4, wherein the encoded region includes at least three solder ball areas.

6. The package of claim 5, wherein the information indicates a voltage supply level for the IC.

7. The package of claim 1, wherein the information indicates a voltage supply level for the IC.

8. An electronic component comprising:

a ball grid array (BGA) package including an encoded region to provide information based upon selective deposition of solder balls; and

a printed circuit board (PCB) coupled to the package.

9. The component of claim 8, wherein the BGA package contains a processor.

10. The package of claim 9, wherein a deposited solder ball in a solder ball area of the encoded region is used to denote a logical "0", and an absence of a solder ball in the solder ball area is used to denote a logical "1".

11. The package of claim 8, wherein any deposited solder ball in a solder ball area of the encoded region is electrically coupled to a first node of a resistor on the PCB, and a second node of the resistor is electrically coupled to a power trace on the PCB.

12. The package of claim 11, wherein the first node is approximately ground if a solder ball is deposited in the solder ball area, and the first node is approximately Vcc if a solder ball is absent from the solder ball area.

13. The package of claim 12, wherein the encoded region includes at least three solder ball areas.

14. The package of claim 13, wherein the information indicates a voltage supply level for a processor within the BGA package.

15. A method of encoding information in an integrated circuit (IC) package, the method comprising:

depositing a first solder ball in a first solder ball area of an encoded region of an IC package to denote a first logical level; and

preventing a solder ball from being deposited in a second solder ball area of the encoded region of the IC package to denote a second logical level.

16. The method of claim 15, wherein depositing the solder ball includes screen printing solder through a template comprising an opening adjacent to the first solder ball area, and preventing a solder ball from being deposited includes screen printing solder through a template comprising a closure adjacent to the second solder ball area,

17. The method of claim 15, further comprising depositing a second solder ball in a third solder ball area of the encoded region of the IC package to denote the first logical level.

18. The method of claim 15, further comprising preventing a solder ball from being deposited in a fourth solder ball area of the encoded region of the IC package to denote the second logical level.